Applicant(s): Stephen J. Battersby et al.
Serial No.: 09/728,189
For: LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURE
Filed: December 01, 2000
Examiner: Akkapeddi, Prasad R.
Group Art Unit: 2871

allowed claims

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (previously presented) A transistor substrate for a liquid crystal display comprising:

a substrate;

a transistor over said substrate, said transistor having an insulated-gate staggered structure with substantially coplanar source and drain regions on said substrate, a gate region, and a gate insulator lying between said gate region and said source and drain regions; and

a capacitor associated with said transistor and lying adjacent thereto, said capacitor having a stacked structure of two electrodes separated by a capacitor dielectric,

wherein said gate region has a first inorganic layer and a second, polymer or spin-on glass layer, of which layers only the polymer or spin-on glass layer extends to said capacitor to define said capacitor dielectric.

2. (original) A transistor substrate as claimed in claim 1, wherein the polymer or spin-on glass layer comprises polyimide.

3. (previously presented) A transistor substrate as claimed in claim 1, wherein the transistor comprises a top gate

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transistor.

4. (currently amended) A liquid crystal display comprising a plurality of pixels provided over a transistor substrate as claimed in ~~any preceding claim~~ claim 1, each pixel comprising respective transistor and capacitor, and wherein the thicknesses of the first and second layers are selected such that the charging time constant of each pixel is invariable to first order changes in the thickness of second polymer or spin-on glass layer defining the capacitor dielectric.

5. (original) A liquid crystal display as claimed in claim 4, wherein, each pixel comprises a capacitor of capacitance C_{store} and is associated with liquid crystal material having a capacitance C_{LC}, wherein the thickness of the inorganic layer d_{inorg} and the thickness of the polymer or spin-on glass layer d_{poly} are selected approximately to satisfy the relation:

$$d_{poly} = (C_{store}/C_{LC}) \cdot (\varepsilon_{poly}/\varepsilon_{inorg}) \cdot d_{inorg}$$

in which ε_{poly} and ε_{inorg} are the permittivity constants of the polymer or spin-on glass layer and the inorganic layer, respectively.

6. (previously presented) A liquid crystal display comprising:

a plurality of pixels each having a switching transistor, a storage capacitor of capacitance C_{store}, and liquid crystal material of capacitance C_{LC}, said transistors having insulated-gate staggered structures with substantially coplanar source and drain regions on said substrate, a gate region, and a gate

insulator lying between said gate region and said source and drain regions, said capacitor having a stacked structure of two electrodes separated by a capacitor dielectric,

wherein said gate region has first and second layers, of which layers only the second extends to said capacitor to define said capacitor dielectric, and wherein the thicknesses of said first and second layers are selected such that the charging time constant of each pixel is invariable to first order changes in the thickness of second layer defining the capacitor dielectric.

7. (original) A display as claimed in claim 6, wherein the thickness of the first layer d_1 and the thickness of the second layer d2 are selected approximately to satisfy the relation:

$$d_2 = (C_{store}/C_{LC}) \cdot (\varepsilon_2/\varepsilon_1) \cdot d_1$$

in which and are the permittivity constants of the first and second layers, respectively.

8. (previously presented) A display as claimed in claim 6, wherein the first layer comprises an inorganic layer, and the second layer comprises a polymer or spin-on glass layer.

9. (original) A display as claimed in claim 8, wherein the second layer comprises polyimide.

10. (previously presented) A method of manufacturing a transistor substrate for a liquid crystal display, comprising providing an array of transistors and capacitors over the substrate, said transistors having insulated-gate staggered

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structures with substantially coplanar source and drain regions, a gate region, and a gate insulator lying between said gate region and said source and drain regions on said substrate; and said capacitors having a stacked structure of two electrodes separated by a capacitor dielectric,

wherein said gate region is deposited as first and second layers, a first layer being deposited by vacuum deposition process, and a second layer being deposited by a non-vacuum process, said first layer being patterned to remove it from areas corresponding to said capacitors, and said second layer extending to the areas corresponding to said capacitors to define said capacitor dielectric.

11. (previously presented) A method of manufacturing a liquid crystal display, comprising manufacturing a transistor substrate using the method of claim 10, and providing liquid crystal material over said transistor substrate,

wherein said first layer is deposited to a thickness d_1, and said second layer is deposited to a thickness d_2, the thicknesses being selected such that the charging time constant of each pixel is invariable to first order changes in the thickness of second layer defining the capacitor dielectric.

12. (original) A method as claimed in claim 11, wherein the capacitors have capacitance C_{store} and each pixel is associated with liquid crystal material of capacitance C_{LC}, and wherein the thickness of the first layer d_1 and the thickness of the second layer d_2 are deposited to depths selected approximately to satisfy the relation:

$$d_2 = (C_{store}/C_{LC}) \cdot (\varepsilon_2/\varepsilon_1) \cdot d_1$$

in which ε_2 and ε_1 are the permittivity constants of the first and second layers, respectively.

13. (previously presented) A transistor substrate as claimed in claim 1, wherein said gate insulator and said first inorganic layer are patterned using the same mask to define a semiconductor island forming a transistor body.